PATENT
Docket No.: M4065.067/P067

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Warren M. Farnworth

Serial No.: Not Yet Assigned

Filed: July 17, 1998

For: TAPED SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE

Assistant Commissioner for Patents
Washington, D.C. 20231

TRANSMITTAL LETTER

Dear Sir:

Enclosed for filing in connection with the above-referenced United States Patent Application are the following:

1. Recordation Form Cover Sheet;
2. Assignment and Agreement;
3. Specification (22 pages);
4. Informal Drawings (5 sheets);
5. Declaration for Patent Application;
6. Power of Attorney by Assignee;

7. Check in the amount of $1,362.00;

8. Two return receipt post cards.

The Commissioner is hereby authorized to charge any fees which may be required in connection with these papers to our Deposit Account 04-1073.

Dated: July 17, 1998

Respectfully submitted,

By _____

Mark J. Thronson
Registration No. 33,082
DICKSTEIN SHAPIRO MORIN
& OSHINSKY LLP
2101 L Street, N.W.
Washington, D.C. 20037-1526
202-785-9700

Attorneys for Applicant

Express Mail Label No.

NEW UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)
(Only for new nonprovisional applications under 37 CFR 1. 53(b))

Docket No.
M4065.067/P067

Total Pages in this Submission

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111 (a) and 37 C.F.R. 1 .53(b) is a new utility patent application for an invention entitled:

TAPED SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE

and invented by:

Warren M. Farnworth

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below

2. ☒ Specification having 22 pages and including the following:

   a. ☒ Descriptive Title of the Invention
   b. ☐ Cross References to Related Applications *(if applicable)*
   c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   d. ☐ Reference to Microfiche Appendix *(if applicable)*
   e. ☒ Background of the Invention
   f. ☒ Brief Summary of the Invention
   g. ☒ Brief Description of the Drawings *(if drawings fled)*
   h. ☒ Detailed Description
   i. ☒ Claim(s) as Classified Below
   j. ☒ Abstract of the Disclosure

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*

   a. ☐ Formal
   b. ☒ Informal

   Number of Sheets 5

NEW UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)
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Docket No.
M4065.067/P067

Total Pages in this Submission

Application Elements (Continued)

4. [x] Oath or Declaration
   a. [x] Newly executed *(original or copy)* [ ] Unexecuted
   b. [ ] Copy from a prior application (37 CFR 1 .63(d)) *(for continuation/divisional application only)*
   c. [ ] With Power of Attorney [x] Without Power of Attorney

5. [ ] Incorporation By Reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is suppliedunder Box 4b, is considered as being part of the disclosure of the accompanying application and is herebyincorporated by reference therein.

6. [ ] Computer Program in Microfiche

7. [ ] Genetic Sequence Submission *(if applicable, all must be included)*
   a. [ ] Paper Copy
   b. [ ] Computer Readable Copy
   c. [ ] Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. [x] Assignment Papers *(cover sheet & documents)*

9. [x] 37 CFR 3.73(b) Statement *(when there is an assignee)*

10. [ ] English Translation Document *(if applicable)*

11. [ ] Information Disclosure Statement/PTO- 1449 [ ] Copies of IDS Citations

12. [ ] Preliminary Amendment

13. [x] Acknowledgment Postcard

14. [ ] Certificate of Mailing
    [ ] First Class [ ] Express Mail *(Specify Label No.):* _____

15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

NEW UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
M4065.067/P067

Total Pages in this Submission

Accompanying Application Parts (Continued)

16. ☐ Additional Enclosures *(please identify below):*

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	33	=	13	x	$22.00	$286.00
Indep. Claims	6	=	3	x	$82.00	$246.00
Multiple Dependent Claims (check if applicable) ☐						0
					BASIC FEE	$790.00
OTHER FEE (specify purpose) Assignment Recordation						$40.00
					TOTAL FILING FEE	$1362.00

☒ A check in the amount of $1362.00 to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. 04-1073. as described below. A duplicate copy of this sheet is enclosed.

☐ Charge the amount of _____ as filing fee.

☒ Credit any overpayment.

☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.

☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311 (b).

Dated: July 17, 1998

Signature

Mark J. Thronson

33,082

PATENT
Docket No.: M4065.067/P067
Micron No.: 98-389

TAPED SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE

Inventor:

Warren M. Farnworth

TAPED SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to taped semiconductor devices. The invention also relates to methods of making taped semiconductor devices. More particularly, the invention relates to a method of making leads on chip (LOC) semiconductor devices with ball grid arrays (BGA).

2. Discussion of the Related Art

A known LOC device is shown in U.S. Patent No. 5,391,918 (Koyanagi et al.). The Koyanagi device has leads located above a semiconductor chip. The leads are separated from the chip by an insulating layer. The leads are connected by wires to bond pads in the center of the chip. The chip, the leads and the wires are encapsulated in a resin package.

The Koyanagi device has a number of disadvantages. One disadvantage is that the leads can be formed on only one chip at a time. To produce the

Koyanagi device, the chip must be singulated from a wafer before the leads are formed. There is a need in the art for an improved method of forming leads on unsingulated chips.

Another disadvantage with the Koyanagi device is that the leads extend laterally beyond the side edges of the chip. The lateral dimensions of the leads are substantially greater than those of the chip. Consequently, the Koyanagi device cannot make efficient use of all of the available space on a printed circuit board.

U.S. Patent No. 5,218,168 (Mitchell et al.) describes a semiconductor device with metal leads formed in a polyimide film. Solder beads connect the leads to respective die circuits and a lead frame. The beads extend through via holes in the polyimide film. A disadvantage with the Mitchell device is that the leads are not applied to the die circuits until after the circuits are diced out of a wafer. The leads are applied separately to singulated semiconductor chips.

Another disadvantage with the Mitchell device is that the lead frame extends beyond the side edges of the chip. Consequently, the area occupied by the finished device is substantially greater than the area available for circuitry on

the chip. Since the periphery of the chip is inside the ends of the leads, the Mitchell device cannot fully utilize space on a printed circuit board.

Another disadvantage with the Mitchell device is that high temperature is used to adhere the polyimide film to the semiconductor chip. The high temperature may cause the film and the chip to expand at different rates, which causes misalignment problems.

SUMMARY OF THE INVENTION

The disadvantages of the prior art are overcome to a great extent by the present invention. In one aspect of the invention, a multi-layer tape is applied to a semiconductor wafer, before the wafer is diced into chips. The tape has a slot-shaped opening for each chip in the wafer. Electrically conductive leads are printed on the tape. Bond wires extend through the openings and connect the chips to the leads. The wires are glob top encapsulated in resin, and ball grid arrays are deposited on the leads. The ball grid arrays are located above the chips, within the respective peripheries of the chips.

In another aspect of the invention, the tape has a dielectric layer, and an adhesive layer is used to connect the dielectric layer to the wafer. Preferably, the

adhesive layer is formed of low temperature curing adhesive material. In a preferred embodiment, the adhesive material achieves ninety percent of its maximum strength in less than about thirty six hours at seventy five degrees Fahrenheit. Consequently, it can be cured at room temperature. The low temperature curing adhesive material avoids misalignment problems that would be caused by a heat activated adhesive.

The adhesive layer may be stenciled onto the wafer before the tape is applied. Alternatively, the adhesive layer is applied to the tape first, and then the adhesive/tape matrix is applied to the wafer. In either event, the tape may be accurately adhered to multiple chips in a single alignment step.

The present invention also relates to a method of making semiconductor devices. The method employs a tape having a dielectric layer and electrically conductive leads. The tape may be stored on a roll. The tape is adhered to the wafer at room temperature to avoid alignment problems caused by differential thermal expansion. Bond wires are formed to connect the integrated circuits on the wafer to the electrically conductive leads.

In another aspect of the invention, the ball grid arrays are formed on the leads before the circuits are diced out of the wafer. This has the advantage of

providing solder balls on a large number of devices at the same time. All of the balls may be formed during a single processing step. In addition, by locating the balls on the leads, inside the periphery of the respective chip, the lateral dimensions of the completed device are no larger than those of the chip. Consequently, space utilization on a printed circuit board is improved. In other words, the amount of chip circuitry and/or memory can be increased per unit area of occupied printed circuit board.

The individual chips may be separated from the wafer by dicing or sawing. During the singulation process, the tape provides mechanical protection for the integrated circuits, and the glob top resin protects the bond wires and the connections at the ends of the bond wires.

In an alternative embodiment of the invention, anisotropically conductive adhesive material is used to form a taped device. In this embodiment, bond wires are replaced by metal located in via holes in the dielectric layer. The anisotropically conductive adhesive material provides electrical connections between the via holes and the bond pads on the chip. The metal in the via holes is integrally connected to leads printed on the tape. A ball grid array is formed on the leads.

These and other features and advantages of the invention will become apparent from the following detailed description of preferred embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a partial plan view of a taped wafer constructed in accordance with the invention.

FIG. 2 is a partial cross sectional view of the taped wafer of FIG. 1, taken along the line 2-2.

FIG. 3 is a partial cross section view, like FIG. 2, showing partially constructed semiconductor devices.

FIG. 4 is a partial cross sectional view, like FIG. 2, showing unsingulated semiconductor devices constructed in accordance with the present invention.

FIG. 5 is a plan view of a mask for dispensing glob top resin.

FIG. 6 is a partial plan view of a semiconductor device constructed in accordance with the invention.

FIG. 7 is a cross section view of the device of FIG. 6, taken along the line 7-7.

FIG. 8 is a partial cross section view of unsingulated semiconductor devices constructed in accordance with another embodiment of the invention..

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Referring now to the drawings, where like reference numerals designate like elements, there is shown in FIG. 1 a semiconductor wafer 10 covered by a printed tape 12. Semiconductor chips 14 are formed in the wafer 10. The wafer 10 is almost entirely covered by the tape 12. Each chip 14 has integrated circuits (not shown) and aligned bond pads 16. The bond pads 16 are electrically connected to the integrated circuits. The tape 12 has slot-shaped openings 18 for exposing the bond pads 16. The tape 12 also has an adhesive layer 20 (FIG. 2), a dielectric layer 22, and leads 24-30. (For clarity of illustration, the leads 24-30 are not shown in FIG. 1.) The openings 18 extend through the adhesive layer 20 (FIG. 2) and the dielectric layer 22.

The adhesive layer 20 may be formed of a low temperature curing material. For example, the adhesive layer 20 may be formed of a two component, room temperature curing epoxy adhesive marketed as Master Bond Polymer System EP31 by Master Bond Inc., of Hackensack, New Jersey. Preferably, the adhesive material cures to ninety percent of its maximum strength within twenty four to thirty six hours at about seventy five degrees Fahrenheit, and to ninety percent of its maximum strength within two to three hours at about one hundred fifty degrees Fahrenheit. The preferred material exhibits low curing shrinkage and reduced stress on the wafer surface 32. Silicone may be added to the adhesive material as a stress relieving agent if desired.

In the illustrated embodiment, the adhesive layer 20 is supplied with the other layers of the tape 12. That is, the adhesive layer 20 is applied to the dielectric layer 22 before the openings 18 are punched through the tape 12. If the adhesive layer 20 is tacky, a backing layer (not shown) may be provided to facilitate handling and storage. In another embodiment of the invention, the adhesive layer 20 is first stenciled onto the wafer surface 32 (without covering the bond pads 16), and then the tape 12 (the dielectric layer 22 and the leads 24-30) is applied onto the adhesive layer 20.

The dielectric layer 22 performs several functions. The dielectric layer 22 provides electrical insulation between the leads 24-30 and the integrated circuits. In addition, the dielectric layer 22 provides mechanical and alpha particle protection for the integrated circuits. In addition, the dielectric layer 22 provides mechanical support for the leads 24-30, before and after the tape 12 is applied to the wafer 10.

In a preferred embodiment of the invention, the dielectric layer 22 includes a layer of polyimide and/or a layer of benzocylobutene (BCB). Polyimide is preferred because it is relatively inexpensive and because it provides protection against alpha particle radiation. Polyimide is a hydrophilic material with high temperature resistance and a high coefficient of thermal expansion. BCB has a high dielectric constant, but it is not as temperature resistant as polyimide. Other materials may be used in the dielectric layer 22, if desired. For example, the dielectric layer 22 may include a layer of KOVAR alloy coated with a suitable polymer, such as polyimide and/or BCB. The polymer material in the dielectric layer 22 is cured before the tape 12 is applied to the wafer 10.

The metal leads 24-30 are preferably formed on the dielectric layer 22, before the tape 12 is applied to the wafer 10.

In operation, the tape 12 is aligned with respect to the wafer 10. The tape 12 is aligned such that the openings 18 are centered over the bond pads 16. The tape 12 may have suitable retention and holding holes 34 (FIG. 1) for facilitating alignment with the wafer 10. All of the integrated circuits on the wafer 10 may be covered by the tape 12 simultaneously.

The adhesive layer 20 (FIG. 2) is cured at low temperature to bond the tape 12 to the wafer 10. A heat source is not required during the bonding step. Curing at low temperature avoids misalignment problems that would otherwise be caused by differential thermal expansion. Preferably, the tape 12 does not expand relative to the top surface 32 of the wafer 10 during the curing of the adhesive layer 20. Preferably, a dielectric material (such as a loaded polyimide) is selected to have a coefficient of thermal expansion which is substantially the same as that of the wafer 10.

Preferably, the adhesive layer 20 is cured to ninety percent of its maximum strength without exceeding one hundred fifty degrees Fahrenheit, even more preferably without exceeding one hundred degrees Fahrenheit. Even more preferably, the temperature of the adhesive layer 20 is maintained at or below room temperature (about seventy five degrees Fahrenheit) throughout the entire bonding process.

Referring now to FIG. 3, after the tape 12 is adhered to the wafer 10, fine bond wires 36, 38 are connected to the bond pads 16 and the leads 24-30. There is one bond wire 36, 38 for each bond pad 16 and printed lead 24-30. (Only two bond wires per chip can be seen in FIG. 3. The other wires are hidden from view in FIG. 3; they are located behind the illustrated bond wires.) Preferably, all of the bond wires 36, 38 for the entire wafer 10 are formed during one processing step. The bond wires 36, 38 may be applied by a Palomar gantry wire bonding machine, for example, or by another suitable device. Suitable equipment may be obtained, for example, from Palomar Products, Inc. of Carlsbad, California.

Then, the bond wires 36, 38, the bond pads 16, and the connections between the bond wires 36, 38 and the leads 24-30 are glob top encapsulated in a suitable resin material 40 (FIG. 4). The resin material 40 provides mechanical protection for the bond wires 36, 38. In addition, the resin material 40 may be hydrophobic to prevent moisture from reaching the bond wires 36, 38. The resin material 40 may be applied through openings 42 (FIG. 5) in a suitable mask 44. There should be one opening 42 for each chip 14 defined in the wafer 10. Retention and holding holes 46 may be provided for aligning the mask 44 with respect to the wafer 10.

Subsequently, minute solder balls 50-56 (FIG. 4) are applied on the respective leads 24-30 to form ball grid arrays (BGA). The balls 50-56 may be applied by a solder ball bumper process, a stencil process, or a preform process. Each ball 50-56 may have a diameter of about 0.325 millimeter. The balls 50-56 provide electrical connections from the leads 24-30 to an exterior device, such as a printed circuit board (not shown). In the illustrated embodiment, all of the balls 50-56 for the entire wafer 10 are applied to the leads 24-30 in a single process step.

The top surfaces 58 of the balls 50-56 should be higher than the top surfaces 60 of the glob top material 40. In the illustrated embodiment, the top surfaces 58 of the balls 50-56 are at least ten mils higher than the top surfaces 60 of the resin material 40. This way, the balls 50-56 are accessible for connection to the exterior device.

The taped and glob topped wafer 10 shown in FIG. 4 is diced or sawed along singulation lines 62 to form individual semiconductor devices 64 (FIGS. 6 and 7). During the singulation process, the tape 12 provides mechanical protection for the wafer surface 32.

In an alternative embodiment of the invention, the wafer 10 may be subdivided into chip clusters (not shown) for certain manufacturing processes. For example, the wafer 10 may be subdivided into chip clusters prior to forming the wires 36, 38, or prior to forming the ball grid arrays 50-56. The entire wafer 10 does not necessarily have to remain in one piece throughout the entire process of manufacturing the semiconductor devices 64.

FIG. 8 shows semiconductor devices 70 constructed in accordance with another embodiment of the invention. The devices 70 are formed by locating a printed tape 72 on a semiconductor wafer 74. Semiconductor chips 76 are formed in the wafer 74. The wafer 74 is covered by the tape 72. Each chip 76 has integrated circuits (not shown) and rows of bond pads 78. The bond pads 78 are electrically connected to the integrated circuits. The tape 72 has via holes 80 located above the bond pads 78. The via holes 80 are formed in a dielectric layer 82. Leads 24-30 are printed on the dielectric layer 82. The leads 24-30 are connected to metal deposited in the via holes 80. Ball grid arrays 50-56 are formed on the leads 24-30 for connection to a printed circuit board or the like.

An anisotropically conductive adhesive layer 84 is used to connect the tape 72 to the wafer 70. The adhesive layer 84 is an electrical conductor in the vertical direction (top to bottom as viewed in FIG. 8). The adhesive layer 84 is

an electrical insulator in horizontal directions. Consequently, the adhesive layer 84 provides electrical connections between the metal in the via holes 80 and the wafer bond pads 78. The adhesive layer 84 otherwise may have the same characteristics and properties as those described above for the adhesive layer 20 shown in FIG. 7. Suitable anisotropically conductive adhesives for the embodiment shown in FIG. 7 are marketed by AI Technology of Princeton, New Jersey, and Zymet of East Hampton, New Jersey.

The dielectric layer 82 shown in FIG. 8 may have the same characteristics and properties as those of the dielectric layer 22 shown in FIG. 7.

The above descriptions and drawings are only illustrative of preferred embodiments which achieve the features and advantages of the present invention, and it is not intended that the present invention be limited thereto. Any modification of the present invention which comes within the spirit and scope of the following claims is considered part of the present invention.

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A semiconductor device, comprising:

a semiconductor chip;

a dielectric layer;

electrically conductive leads on said dielectric layer; and

a low temperature curing adhesive material between said semiconductor chip and said dielectric layer.

2. The semiconductor device of claim 1, wherein said dielectric layer includes polyimide.

3. The semiconductor device of claim 1, wherein said dielectric layer includes benzocylobutene.

4. The semiconductor device of claim 1, further comprising bond wires connecting said semiconductor chip to said electrically conductive leads.

5. The semiconductor device of claim 4, further comprising resin material encapsulating said bond wires.

6. The semiconductor device of claim 5, further comprising an opening defined in said dielectric layer, and wherein said bond wires and said resin material are located in said opening.

7. The semiconductor device of claim 6, further comprising a ball grid array on said leads.

8. A taped semiconductor product, comprising:

integrated circuits formed in semiconductor material;

a tape having openings aligned with said integrated circuits;

bond wires extending through said openings, said bond wires being electrically connected to said integrated circuits; and

adhesive material between said tape and said integrated circuits.

9. The taped semiconductor product of claim 8, wherein said tape includes a dielectric layer and electrically conductive leads, said leads being printed on said dielectric layer.

10. The taped semiconductor product of claim 9, wherein said adhesive material cures at room temperature.

11. The taped semiconductor product of claim 10, further comprising glob top encapsulant material in said openings.

12. The taped semiconductor product of claim 11, further comprising a ball grid array for each of said integrated circuits, said ball grid arrays being located on said electrically conductive leads.

13. A tape for manufacturing semiconductor devices, said tape comprising:

a dielectric layer having openings;

electrically conductive leads associated with said openings, said leads being printed on said dielectric layer; and

a low temperature curing adhesive material.

14. The tape of claim 13, wherein said dielectric material includes polyimide.

15. The tape of claim 13, wherein said dielectric material includes benzocylobutene.

16. The tape of claim 13, wherein said dielectric material includes a metal alloy and a polymer coating.

17. The tape of claim 13, wherein said openings are slot-shaped to expose aligned bond pads.

18. The tape of claim 17, wherein said openings are punched through said dielectric layer.

19. A method of making semiconductor devices, said method comprising the steps of:

providing a semiconductor product having integrated circuits;

providing a tape having a dielectric layer and electrically conductive leads;

adhering said tape to said semiconductor product at low temperature; and

electrically connecting said integrated circuits to said electrically conductive leads.

20. The method of claim 19, wherein the temperature of said tape does not exceed one hundred fifty degrees Fahrenheit during said adhering step.

21. The method of claim 20, wherein said step of electrically connecting said integrated circuits to said leads includes the step of connecting bond wires to bond pads on said semiconductor product.

22. The method of claim 21, further comprising the step of locating ball grid arrays on said electrically conductive leads.

23. The method of claim 22, further comprising the step of encapsulating said bond wires in resin.

24. The method of claim 23, further comprising the step of dicing said semiconductor product to separate said integrated circuits into individual semiconductor chips.

25. A method of making taped products, said method comprising the steps of:

providing a sheet having electrically conductive leads and an epoxy adhesive layer;

aligning said sheet with respect to integrated circuits; and

curing said adhesive layer at low temperature.

26. The method of claim 25, further comprising the step of connecting wires to said integrated circuits and said electrically conductive leads.

27. The method of claim 26, wherein the temperature of said adhesive layer does not exceed one hundred degrees Fahrenheit during said curing step.

28. The method of claim 27, further comprising the step of connecting ball grid arrays to said leads.

29. The method of claim 28, further comprising the step of flowing resin through a mask to glob top encapsulate said wires.

30. The method of claim 29, further comprising the step of separating said integrated circuits from each other to produce integrated circuit devices.

31. A semiconductor device, comprising:

a semiconductor chip;

a dielectric layer;

electrically conductive leads on said dielectric layer; and

an anisotropically conductive adhesive material located between said dielectric layer and said semiconductor chip.

32. The semiconductor device of claim 31, further comprising via holes defined in said dielectric layer, and metal located in said via holes, said metal being connected to said leads.

33. The semiconductor device of claim 32, further comprising a ball grid array on said leads, said ball grid array being located within the periphery of said chip.

ABSTRACT

Printed tape is used to form a leads on chip (LOC) ball grid array (BGA) semiconductor device. Leads for a plurality of devices may be applied simultaneously. Bond wires, glob top encapsulant, and the ball grid arrays for the devices may be formed in single process steps. A low temperature curing adhesive material may be used to reduce the effects of differential thermal expansion between the tape and surface of the wafer. In another embodiment of the invention, anisotropically conductive adhesive material is used to connect bond pads on a wafer to leads printed on a tape.

Fig. 1

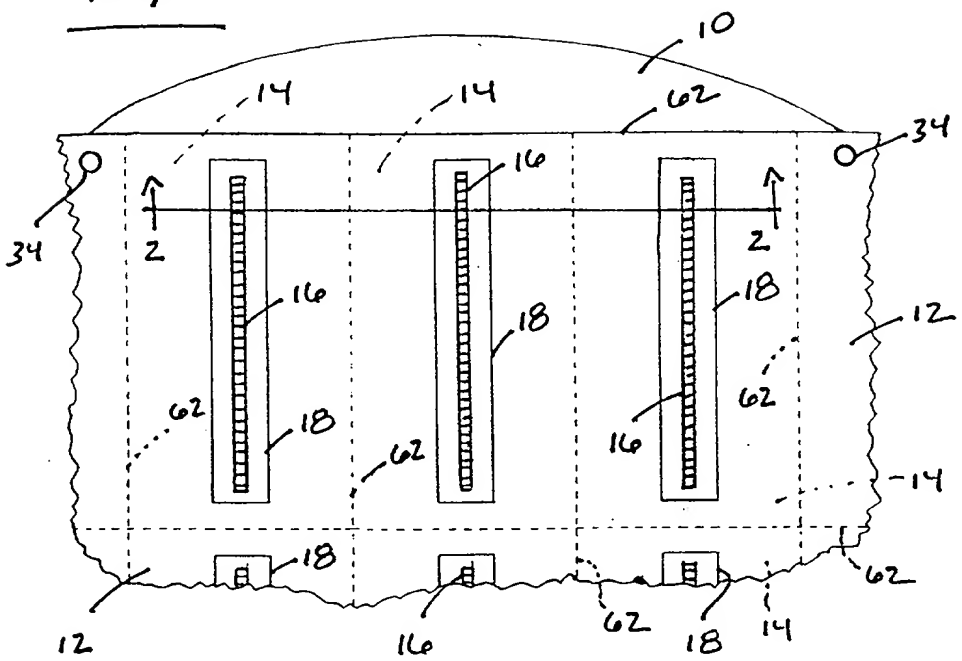
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Fig. 2

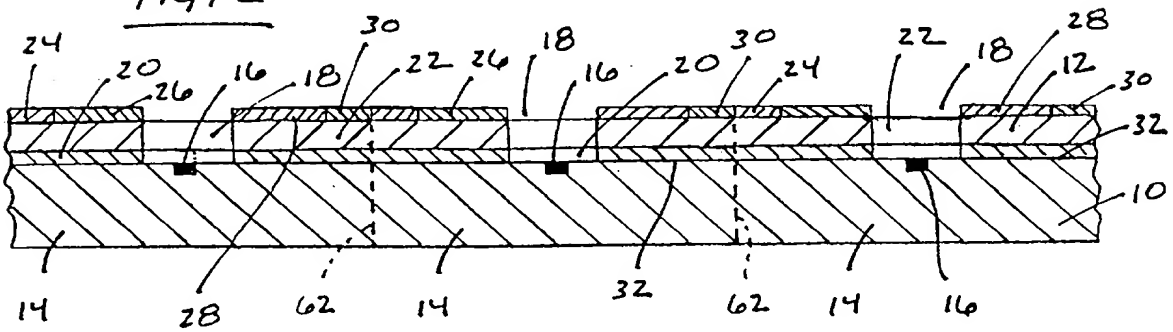
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Fig. 3

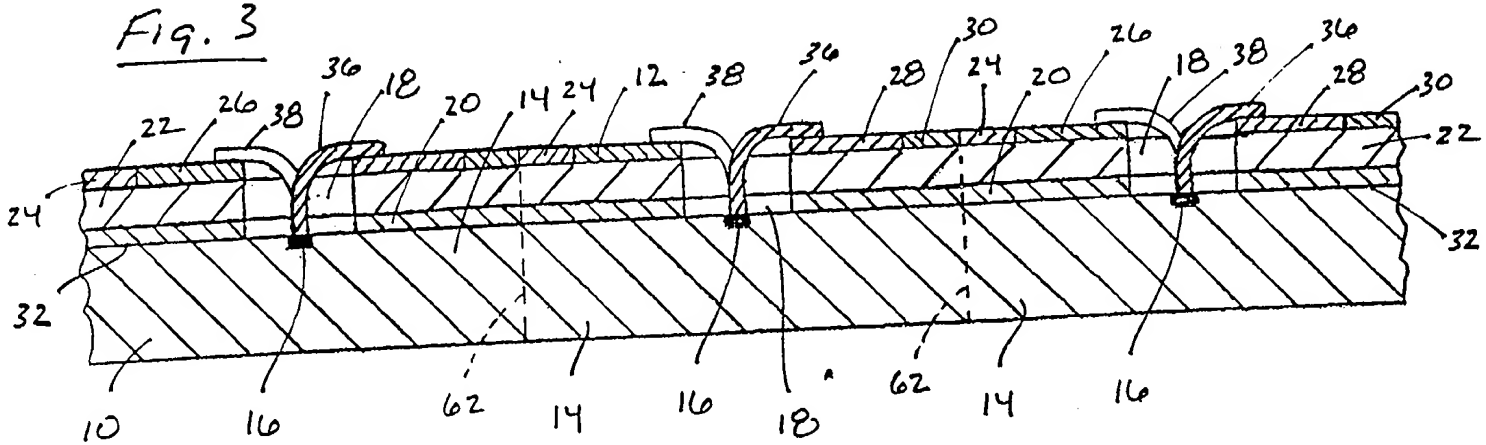
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Fig. 4

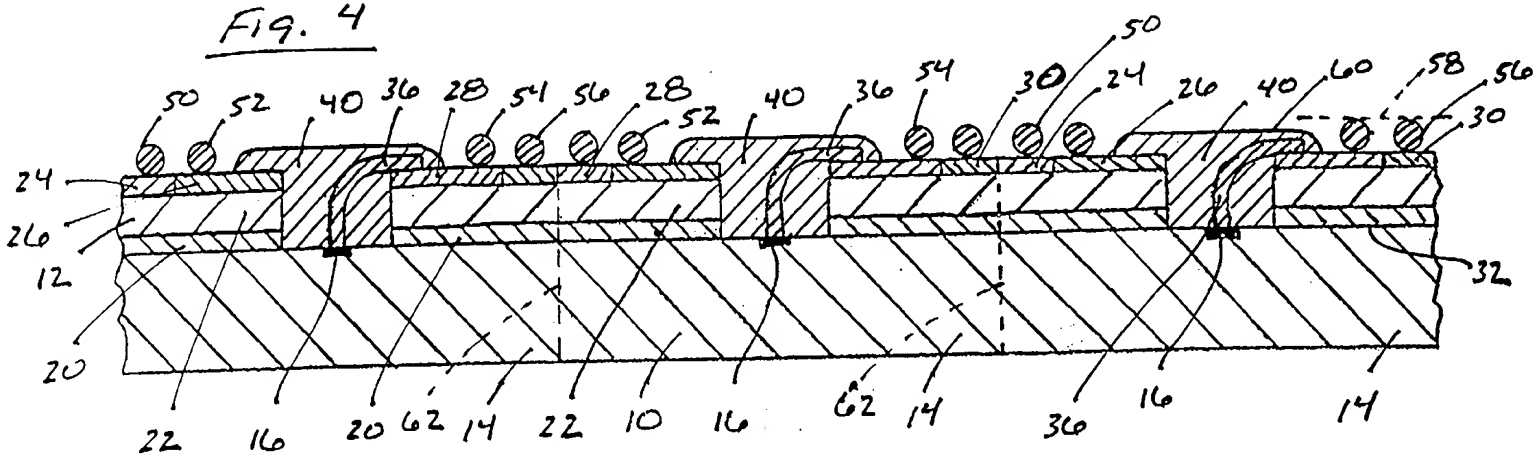
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Fig. 5

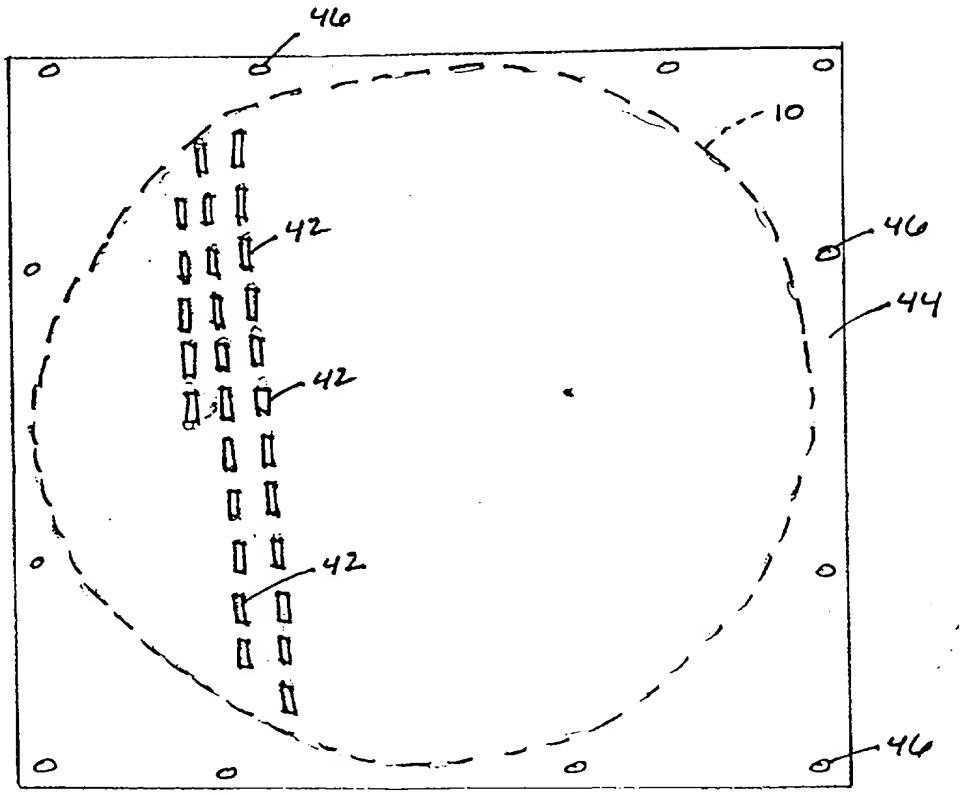


Fig. 6

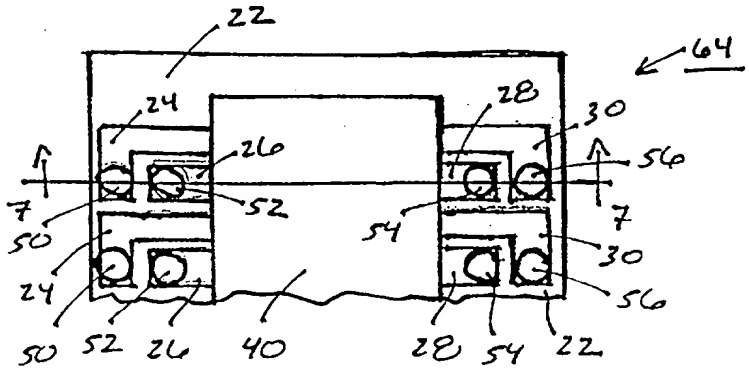


Fig. 7

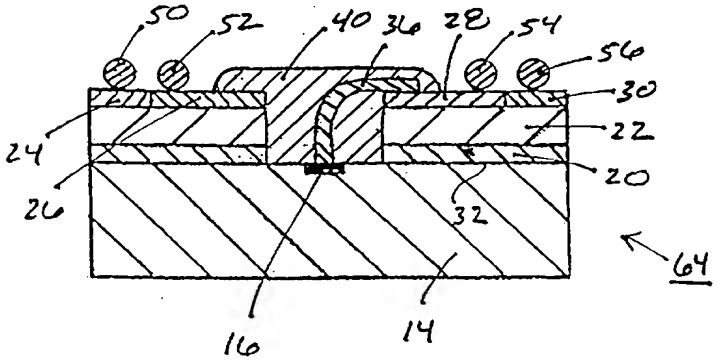
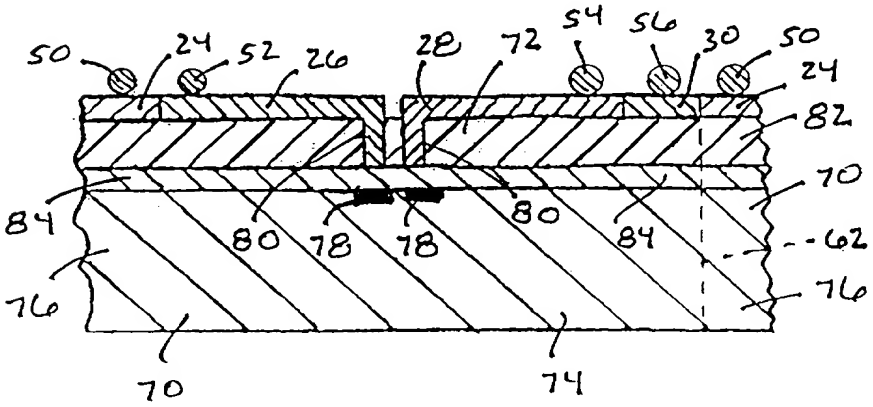


Fig. 8



Docket No.: M4065.067/P067
Micron No.: 98-389

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECLARATION FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

TAPED SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

None

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

None

Docket No.: M4065.067/P067
Micron No.: 98-389

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Please address all correspondence to Thomas J. D'Amico of Dickstein Shapiro Morin & Oshinsky LLP, located at 2101 L Street, NW, Washington, DC 20037-1526. Telephone calls should be made to Thomas J. D'Amico by dialing (202) 828-2232.

Full name of sole inventor: Warren M. Farnworth

Inventor's signature Warren Farnworth Date 7-15-1998

Residence: Nampa, Idaho

Citizenship: United States of America

Post Office Address: 2004 S. ~~Banna~~ Banner, Nampa, Idaho 83686

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PATENT
Docket No.: M4065.067/P067
Micron No.: 98-389

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

Patent Application
Inventor: Warren M. Farnworth

Serial No.: Not Yet Assigned — Group Art Unit: Not Yet Assigned

Filed: Concurrently Herewith — Examiner: Not Yet Assigned

For: TAPED SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE

POWER OF ATTORNEY BY ASSIGNEE AND

CERTIFICATE BY ASSIGNEE UNDER 37 CFR § 3.73(b)

Micron Technology, Inc., assignee of the entire right, title and interest in the above-identified application by virtue of the assignment attached hereto (which is also being submitted concurrently for recordation), hereby appoints the attorneys and agents of the firm of Dickstein Shapiro Morin & Oshinsky LLP, located at 2101 L Street, NW, Washington, DC 20037-1526, listed as follows: Gary M. Hoffman, 26,411; Thomas J. D'Amico, 28,371; Donald A. Gregory, 28,954; James W. Brady, Jr., 32,115; Jon D. Grossman, 32,699; Mark J. Thronson, 33,082; Laurence D. Fisher, 37,131; John R. Fuisz, 37,327; Juliana Haydoutova, P43,313; James M. Heintz, P41,828; Herbert V. Kerner, P42,721; Gianni Minutoli, 41,198; Eric Oliver, 35,307; William E. Powell, III, 39,803; James M. Silbermann, 40,413; Richard Veltman, 36,957 and Darius

Gambino, 41,472, and also attorneys Michael L. Lynch, 30,871; Lia M. Pappas, 34,095; W. Eric Webostad, 35,406; and Charles B. Brantley, II, 38,086 of Micron Technology, Inc. as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The assignee certifies that the above-identified assignment has been reviewed and to the best of the assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to the following:

Thomas J. D'Amico, Esq.
Dickstein Shapiro Morin & Oshinsky LLP
2101 L Street, NW
Washington, D.C. 20037-1526
Telephone: (202) 828-2232
Facsimile: (202) 887-0689

MICRON TECHNOLOGY, INC.

Michael L. Lynch
Chief Patent Counsel
Registration No. 30,871

Dated: 2/16/1998